ISSUE 1 May 1995

## Features

- Receive sync output pulse
- Full duplex transmission over a single twisted pair
- Selectable 80 or 160 kbit/s line rate
- Adaptive echo cancellation
- Up to 4 km loop reach
- ISDN compatible (2B+D) data format
- Transparent modem capability
- Frame synchronization and clock extraction
- MITEL ST-BUS compatible
- Low power (typically 50 mW), single 5V supply

## Applications

- TDD Digital PCS (DECT, CT2, PHS) base stations requiring cell synchronization
- Digital subscriber lines
- High speed data transmission over twisted wires
- Digital PABX line cards and telephone sets
- 80 or 160 kbit/s single chip modem

**Ordering Information**

| | |
|---|---|
| MT9174AE | 24 Pin Plastic DIP |
| MT9174AN | 24 Pin SSOP |
| MT9174AP | 28 Pin PLCC |

**-40°C to +85°C**

## Description

The MT9174 is identical to the MT9172 in all respects except for the addition of one feature. The MT9174 includes a digital output pin indicating the temporal position of the "SYNC" bit of the biphase transmission. This feature is especially useful for systems such as PCS wireless base stations applications requiring close synchronization between microcells.

The MT9174 is fabricated in Mitel's ISO$^2$-CMOS process.

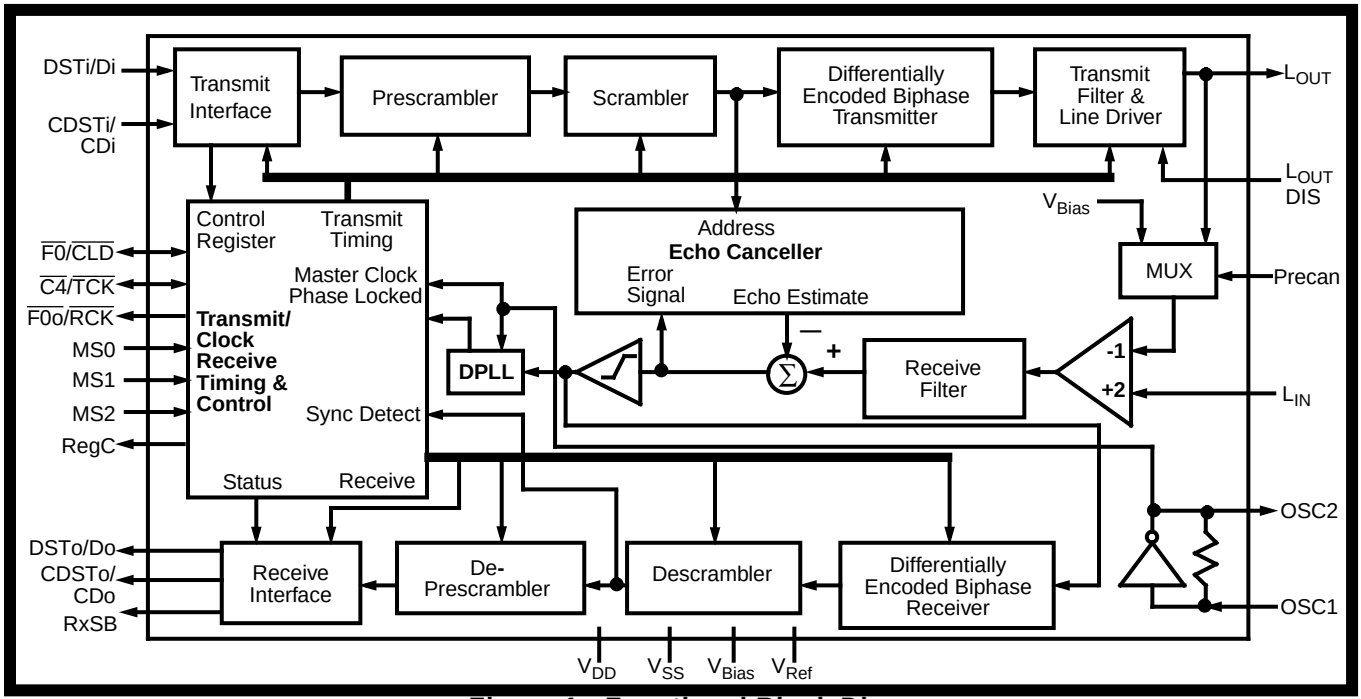


**Figure 1 - Functional Block Diagram**

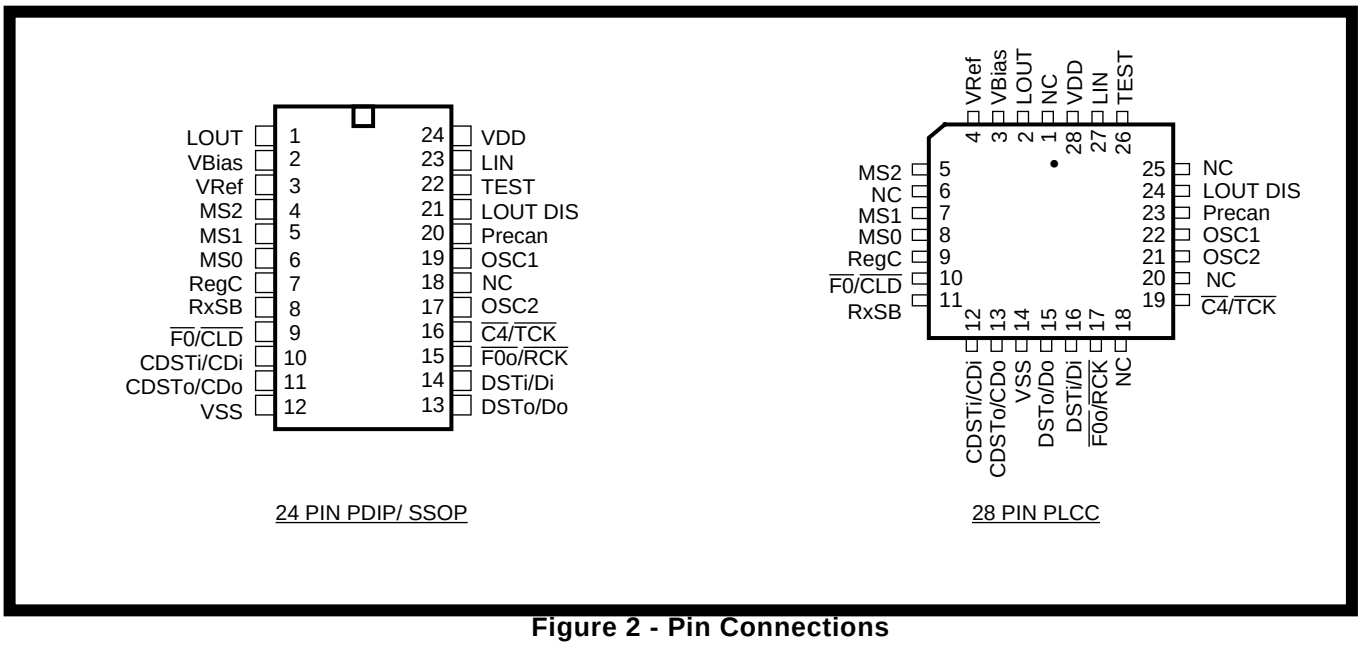


**Figure 2 - Pin Connections**

## Pin Description

| Pin # | | Name | Description |
|---|---|---|---|
| **24** | **28** | | |
| 1 | 2 | $L_{OUT}$ | **Line Out.** Transmit Signal output (Analog). Referenced to $V_{Bias}$. |
| 2 | 3 | $V_{Bias}$ | **Internal Bias Voltage** output. Connect via 0.33 µF decoupling capacitor to $V_{DD}$. |
| 3 | 4 | $V_{Ref}$ | **Internal Reference Voltage** output. Connect via 0.33 µF decoupling capacitor to $V_{DD}$. |
| 4,5, 6 | 5,7, 8 | MS2-MS0 | **Mode Select** inputs (Digital). The logic levels present on these pins select the various operating modes for a particular application. See Table 1 for the operating modes. |
| 7 | 9 | RegC | **Regulator Control** output (Digital). A 512 kHz clock used for switch mode power supplies. Unused in MAS/MOD mode and should be left open circuit. |
| 8 | 11 | RxSB | **Receive Sync Bit** output (Digital). This output is held high until receive synchronization occurs (i.e., until the sync bit in Status Register =1). Once low, indicating synchronized transmission, a high going pulse (6.24 µs wide pulse @ 160 kb/s and 12.5 µs wide @ 80 kb/s) indicates the temporal position of the receive "SYNC" bit in the biphase line transmission. |
| 9 | 10 | F0/CLD | **Frame Pulse/C-Channel Load** (Digital). In DN mode a 244 ns wide negative pulse input for the MASTER indicating the start of the active channel times of the device. Output for the SLAVE indicating the start of the active channel times of the device. Output in MOD mode providing a pulse indicating the start of the C-channel. |
| 10 | 12 | CDSTi/ CDi | **Control/Data ST-BUS In/Control/Data In** (Digital). A 2.048 Mbit/s serial control & signalling input in DN mode. In MOD mode this is a continuous bit stream at the bit rate selected. |
| 11 | 13 | CDSTo/ CDo | **Control/Data ST-BUS Out/Control/Data Out** (Digital). A 2.048 Mbit/s serial control & signalling output in DN mode. In MOD mode this is a continuous bit stream at the bit rate selected. |
| 12 | 14 | $V_{SS}$ | **Negative Power Supply** (0V). |
| 13 | 15 | DSTo/Do | **Data ST-BUS Out/Data Out** (Digital). A 2.048 Mbit/s serial PCM/data output in DN mode. In MOD mode this is a continuous bit stream at the bit rate selected. |
| 14 | 16 | DSTi/Di | **Data ST-BUS In/Data In** (Digital). A 2.048 Mbit/s serial PCM/data input in DN mode. In MOD mode this is a continuous bit stream at the bit rate selected. |

## Pin Description (continued)

| Pin # | | Name | Description |
|---|---|---|---|
| **24** | **28** | | |
| 15 | 17 | $\overline{F0o}/\overline{RCK}$ | **Frame Pulse Out/Receive Bit Rate Clock** output (Digital). In DN mode a 244 ns wide negative pulse indicating the end of the active channel times of the device to allow daisy chaining. In MOD mode provides the receive bit rate clock to the system. |
| 16 | 19 | $\overline{C4}/\overline{TCK}$ | **Data Clock/Transmit Baud Rate Clock** (Digital). A 4.096 MHz TTL compatible clock input for the MASTER and output for the SLAVE in DN mode. For MOD mode this pin provides the transmit bit rate clock to the system. |
| 17 | 21 | OSC2 | **Oscillator Output**. CMOS Output. |
| 19 | 22 | OSC1 | **Oscillator Input**. CMOS Input. D.C. couple signals to this pin. Refer to D.C. Electrical Characteristics for OSC1 input requirements. |
| 20 | 23 | Precan | **Precanceller Disable.** When held to Logic '1', the internal path from $L_{OUT}$ to the precanceller is forced to $V_{Bias}$ thus bypassing the precanceller section. When logic '0', the $L_{OUT}$ to the precanceller path is enabled and functions normally. An internal pulldown (50 kΩ) is provided on this pin. |
| 18 | 1,6, 18, 20, 25 | NC | **No Connection.** Leave open circuit |
| 21 | 24 | $L_{OUT}$ DIS | **$L_{OUT}$ Disable.** When held to logic "1", $L_{OUT}$ is disabled (i.e., output = $V_{Bias}$). When logic "0", $L_{OUT}$ functions normally. An internal pulldown (50 kΩ) is provided on this pin. |
| 22 | 26 | TEST | **Test Pin.** Connect to $V_{SS}$. |
| 23 | 27 | $L_{IN}$ | **Receive Signal** input (Analog). |
| 24 | 28 | $V_{DD}$ | **Positive Power Supply** (+5V) input. |

**Notes:**